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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/566,529	06/05/2006	Stephan Bolz	S4-03P04584	5910	
24131	7590	07/02/2008			
LERNER GREENBERG STEMER LLP		EXAMINER			
P O BOX 2480		CLARK, CHRISTOPHER JAY			
HOLLYWOOD, FL 33022-2480		ART UNIT		PAPER NUMBER	
		2836			
		MAIL DATE		DELIVERY MODE	
		07/02/2008		PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

**DETAILED ACTION**

***Response to Arguments***

1. Applicant's arguments filed May 27, 2008 have been fully considered but they are not persuasive.
2. The applicant argues that there is no need to provide a diode because there is no large resistance to bypass. The examiner respectfully disagrees. As disclosed previously, Williams teaches placing a diode in parallel with a resistor that is attached to the gate of a transistor so that the transistor may turn off at a faster rate. Though the resistor as disclosed in Williams may be of a large value, the teaching of Williams still conveys to one of ordinary skill in the art that by placing a diode in parallel with a resistor connected to the gate of a transistor, the turn off time of the transistor can be reduced in comparison with the turn on time. One skilled in the art would find this a desirable result especially in an application as taught by Gscheidle where it would be desirable for the transistor T2 to switch off as soon as possible when an over voltage condition is detected.
3. Furthermore, the applicant argues that by bypassing the resistor R4, the current flowing through transistor T1 may cause damage and one skilled in the art would not which to do so. The examiner respectfully disagrees. There is no indication in the disclosure of Gscheidle that R4 is required in order to limit current so that T1 may be protected. In fact Gscheidle states that R4 is included in order to generate gate bias to T2, which would not be affected by the addition of the aforementioned diode (Column 3 Lines 61-64). One skilled in the art would also realize that many transistors such as T1 are designed to handle a high current capability. One skilled in the art would also understand that the majority of current that flows through T1 when it is

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activated comes from the battery "Ubatt" which has its current limited by R3 and very little current flows from the gate of T2. Also, even if T1 were to become at risk, if one skilled in the art deemed it necessary to increase the speed of turn off in order to provide the protection needed, they may find the consequences of damaging transistor T1 minor compared to the importance of providing a more rapidly responding protection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER J. CLARK whose telephone number is (571)270-1427. The examiner can normally be reached on M-F, 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/  
Supervisory Patent Examiner, Art Unit 2836

CJC

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